Notice of Allowability	Application No.	Applicant(s)	
	09/712,246	TANIZAKI ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/14/2005*.

2. ☒ The allowed claim(s) is/are *19 and 20*.

3. ☒ The drawings filed on *15 November 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *8/23/2005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

8/23/05

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Tomoki Tanida (202-756-8196) on August 23, 2005.

The application has been amended as follows:

Please cancel claim 17.

Please cancel claim 18.

Please replace 19 with:

A method of providing data read out from a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a second frequency lower than said first frequency, wherein the ratio of said first frequency to said second frequency is a predetermined positive integer, said method comprising the step of: repeating for a plurality, identical to said predetermined positive integer, of times sequential output of a plurality of data items read out from said memory cell array one

by one per one cycle of said first clock signal, said plurality of data items constituting a data block repeatedly read out one by one per one cycle of said second clock signal for said plurality of times.

REASONS FOR ALLOWANCE

Claims 19 and 20 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 19 of the present application teaches method of providing data read out from a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a second frequency lower than said first frequency, wherein the ratio of said first frequency to said second frequency is a predetermined positive integer, said method comprising the step of: repeating for a plurality, identical to said predetermined positive integer, of times sequential output of a plurality of data items read out from said memory cell array one by one per one cycle of said first clock signal, said plurality of data items constituting a data block repeatedly read out one by one per one cycle of said second clock signal for said plurality of times. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Lepejian, teaches a built-in self test circuit for an integrated circuit tests one or more embedded memories by writing data to each memory address, reading it back out, and then comparing the input and output data to see if they match. The BIST circuit includes one or more data generators for supplying a sequence of data to be written to the various addresses of each memory and one or more identical address

generators, each for supplying addresses to a separate embedded memory during read and write operations. Though the memories may have differently sized address spaces, all address generators generate a similar address sequence having a range of address values as large or larger than the address space of the largest memory. During each memory write cycle, a separate filter checks the address output of each address generator to determine whether the address is within the address space of the corresponding memory. If so, the BIST circuit writes the current data output of a data generator to that address of the memory. If not, the BIST circuit ignores the current address and data outputs of the address and data generators and repeats the write operation it performed during a next preceding memory write cycle, writing the same data to the same valid memory address. The BIST circuit makes a similar address substitution during write operation. This allows the BIST circuit to use identical address generators for all memories regardless of the size of the memory being tested. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 19 of the present application. In particular, the limitations of "...a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a second frequency lower than said first frequency, wherein the ratio of said first frequency to said second frequency is a predetermined positive integer, said method comprising the step of: repeating for a plurality, identical to said predetermined positive integer, of times sequential output of a plurality of data items read out from said memory cell array one by one per one cycle of said first clock signal, said plurality of data items constituting a data block repeatedly read out one by one per one cycle of said second clock signal for said plurality of times." are not taught nor fairly suggested in the prior arts of record.

Dependent claim 20 depends from independent claim 19 and inherently includes limitations therein and therefore is allowed as well.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
August 23, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100